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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* ANDREW MARK NIGHTINGALE

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Appeal 2009-002116
Application 10/764,495
Technology Center 2100

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Before THOMAS S. HAHN, ELENI MANTIS MERCADER, and CARL W. WHITEHEAD, JR., *Administrative Patent Judges*.

HAHN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant invokes our review under 35 U.S.C. § 134(a) from a final rejection of claims 1-51. We have jurisdiction under 35 U.S.C. § 6(b). An oral hearing was held on October 18, 2011. We reverse.

## STATEMENT OF THE CASE

### *Introduction*

Appellant claims a verification testing apparatus and method for a combined hardware and software system. The claims recite coordinating verification testing through sequencing execution of software routines with hardware testing by having a test manager connected through both a debugger signal interface controller and a debugger to control a processing unit.[1] The below reproduced claim 1 is illustrative:

> 1. Apparatus for performing a sequence of verification tests to perform hardware and software co-verification on a system under verification, comprising:
>
> a plurality of signal interface controllers operable to be coupled to said system under verification, each signal interface controller being operable to perform one or more test actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of the system under verification and said signal interface controller during performance of said sequence of verification tests;
>
> a debugger operable to control operation of a processing unit associated with the system under verification, the processing unit being operable to execute software routines;
>
> a debugger signal interface controller operable to interface with the debugger and to perform one or more test actions transferring at least one of one or more stimulus signals and one or more response signals between the debugger and said debugger signal interface controller during performance of said sequence of verification tests; and

[1] *See generally* Spec. 2:22-25, 14:16-22, 15:11–16:22; Fig. 3.

> a test manager coupled to said plurality of signal interface controllers and the debugger signal interface controller and operable to transfer test controlling messages to said plurality of signal interface controllers and the debugger signal interface controller identifying the test actions to be performed;
>
> the test manager being operable to control the operation of the processing unit via the debugger signal interface controller and the debugger in order to co-ordinate the execution of said software routines with the sequence of verification tests.

*Rejections*

The Examiner rejected claims 1-51 under 35 U.S.C. § 101 as being directed to non-statutory subject matter (Final Action 3-4).

The Examiner also rejected claims 1-51 under 35 U.S.C. § 102(e) as being anticipated by Rajsuman (US 6,678,645 B1; Jan. 13, 2004) (Final Action 4-19).

*Appellant's Contentions*

Appellant contends the claims recite statutory subject matter because they "accomplish a practical application . . . that provides a useful, concrete, and tangible result" (App. Br. 7).

Appellant, with respect to the rejection under 35 U.S.C. § 102(e), contends Rajsuman is a deficient anticipation reference because "Rajsuman lacks the coordinated execution of the claimed software routines along with the sequence of hardware verification tests made possible with the claimed debugger and debugger interface controller" (App. Br. 14).

*Issues on Appeal*

Did the Examiner err under 35 U.S.C. § 101 by concluding that the claimed subject matter is non-statutory because, as construed, it fails to provide any useful, concrete, or tangible result?

Did the Examiner err under 35 U.S.C. § 102(e) in rejecting claims 1-51 because Rajsuman explicitly or inherently fails to teach coordinating verification testing through sequencing execution of software routines with hardware testing by having a test manager connected through both a debugger signal interface controller and a debugger to control a processing unit?

## ANALYSIS

### *Statutory Subject Matter*

We reviewed the Examiner's rejection under 35 U.S.C. § 101 in light of Appellant's argument for patentability referenced *supra*, and we agree with Appellant's conclusion that the Examiner erred.

The Examiner indicates for the rejection that:

> [T]he claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible result. The Examiner asserts that the claims do not indicate if the methods or apparatus are tangible methods or apparatus utilizing hardware, instead of an arrangement of software lacking tangible embodiment. Further, following Applicant[']s amendment claim 35 recites an intended use. The phrase "for use in" in claim 35 is an intended use and therefore the limitations following said phrase are not afforded patentable weight.

(Ans. 3). Appellant disagrees and contends that the claimed subject matter does provide useful, concrete, or tangible results (App. Br. 7-10; Reply Br. 1-3). To support this contention, Appellant asserts that:

- Claim 1 recites apparatus elements that include

> signal interface controllers coupled to the system under verification, a processing unit that executes software routines, a debugger that controls the processing unit, a

> debugger signal interface controller that causes stimulus and response signals to be exchanged . . . , and a test manager that accomplish[es] the hardware and software co-verification on a system under verification.

(App. Br. 8);

- Claim 18 recites a method for "physically testing a system using 'signal interface controllers' and 'controlling via a debugger execution of software routines by a processing unit associated with the system under verification'" (*id.*); and
- Claim 35 recites

> "a computer program product embodied on a computer-readable medium for use in performing a sequence of verification tests to perform hardware and software co-verification on a system under verification" . . . [so] that [the] program code causes a computer to perform the recited tasks for performing a sequence of verification tests to perform coordinated hardware and software testing.

(App. Br. 9).

The Examiner is silent concerning these asserted interpretations and quotations of claimed subject matter.

The Examiner, however, responds by categorically indicating that according to Appellant's Specification "elements of the claims . . . can be implemented in either hardware or software and as such the claims result in software per se which is not patentable" (Ans. 19). Appellant next responds by continuing in contending that the claims recite statutory subject matter (Reply Br. 1-3). To support the repeated contention, Appellant quotes Specification disclosures describing computer hardware that can execute software (Reply Br. 1-2; *see* Specification 21:3-21). Further, Appellant argues with the explanation that "the invention yields a useful, concrete, and

tangible result – the co-verification of hardware and software on a system under verification . . . ." (Reply Br. 2).

Based on our review of the record, we find that all of the independent claims 1, 18, and 35 recite elements directed to co-verification testing of system hardware and software. As such, we find these claims recite apparatus and method elements that yield useful, concrete, and tangible results, e.g., co-verification testing of system hardware and software. Further, we do not find these claims exclusively reciting "software per se" (Ans. 19) because they recite, *inter alia*, including and using a processing unit, i.e., a computer, that has hardware devices, which are capable of executing and being directed by software (Reply Br. 1-2; *see* Spec. 21:3-21). Accordingly, we do not sustain the rejection under 35 U.S.C. § 101 of claims 1-51.

*Anticipation*

We reviewed the Examiner's rejection under 35 U.S.C. § 102(e) in light of Appellant's argument for patentability referenced *supra*, and we agree with Appellant's conclusion that the Examiner erred.

Appellant contends that:

> Th[e] claimed functionality is not directed to detecting faults in the claimed processing unit, but instead to synchronizing hardware and software activities, thereby enabling a sequence of verification tests to be performed to test for the correct operation of the software and hardware of the system in combination. Rajsuman lacks the coordinated execution of the claimed software routines along with the sequence of hardware verification tests made possible with the claimed debugger and debugger interface controller.

(App. Br. 14). The Examiner responds with citations and quotes from Rajsuman (Ans. 19-20), and indicates that "the reference generates test

pattern signals for debugging a fault which reads on the limitation as recited" (Ans. 20). The Examiner does not indicate what is the referred-to limitation.

From our review of the record, we do not find Appellant and the Examiner disputing what is taught in Rajsuman, but, instead, we find the dispute concerns whether the reference explicitly or inherently teaches a claimed limitation. According to Appellant the disputed limitation is "[t]he claimed debugger [being] used with a debugger signal interface controller to provide the test manager with a mechanism for gaining control over the software executing on the CPU, and in this way, provid[ing] the test manager with a mechanism to synchronize hardware and software activities" (Reply Br. 5). In the Reply Brief Appellant solely relies on claim 1 and asserts that the submitted arguments also apply to the other independent claims (Reply Br. 3); we agree that the same disputed limitation is substantively recited in all of the independent claims.[2]

The Examiner finds Rajsuman teaches generating test pattern signals for debugging a fault (Ans. 20), but is silent concerning a test manager controlling a processing unit. Based on our review of the record, we do not find Rajsuman explicitly or inherently teaches coordinating verification testing through sequencing execution of software routines with hardware testing by having a test manager connected through both a debugger signal interface controller and a debugger to control a processing unit.

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[2] The disputed limitation as recited in claim 1 reads a "test manager being operable to control the operation of [a] processing unit via [a] debugger signal interface controller and [a] debugger in order to co-ordinate the execution of . . . software routines with [a] sequence of verification tests."

We consequently agree with Appellant that not all independent claim limitations are taught in Rajsuman, and, therefore, the rejected claims are not anticipated. *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (An anticipation reference must teach every claimed element.).

For the foregoing reasons we do not sustain the rejection of independent claims 1, 18, and 35. For the same reason we also do not sustain the anticipation rejection of dependent claims 2-17, 19-34, and 36-51.

## CONCLUSIONS

1. The Examiner erred under 35 U.S.C. § 101 by concluding that the claimed subject matter is non-statutory because when properly construed the claimed subject matter provides a useful, concrete, and tangible result.
2. The Examiner erred under 35 U.S.C. § 102(e) in rejecting claims 1-51 because Rajsuman teaches the claimed coordinating verification testing through sequencing execution of software routines with hardware testing by having a test manager connected through both a debugger signal interface controller and a debugger to control a processing unit.
3. This record does not show that claims 1-51 are unpatentable.

## ORDER

The Examiner's rejections of claims 1-51 are reversed.

REVERSED

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